eRD104 Project R&D Proposal for FY23

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EIC Silicon Consortium

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1 Silicon Services Reduction

The overarching goal of the EIC Silicon Consortium is the development and construction of a full tracking and vertexing detector subsystem for the EIC detector(s). This requires R&D in multiple areas, including service reduction which forms the topic of this proposal. Silicon tracking detector services reduction efforts are concentrated in the areas where the bulk of the detector services exists. Specifically in the powering system and the readout system. While the specifics of the R&D and prototyping in this proposal will be formulated for the silicon tracking powering and readout systems, we welcome working with other detector subsystems on services reductions in these areas. Commonality of components over detector subsystems is a useful attribute.

1.1 Powering System

By far the largest component of services for the silicon tracking detector in traditional (ALICE ITS2 like) configurations is the powering system cabling. The goal of this R&D is to investigate the possibilities of serial powering, possibly with on-chip regulation and/or the use of on detector radiation tolerant DC-DC converters. These powering system architectures could reduce the material from power cables substantially.

1.2 Readout System

The readout cabling for the silicon tracking detector, currently projected to consist of Samtec Twinax, also is a significant fraction of the servicing load required for the detector. In this R&D topic we will investigate the use cases and possible topologies and technological solutions for a multiplexing system based on radiation tolerant FPGAs to aggregate the data from the sensor outputs and transmit this aggregated data outside of the detector volume on high speed optical links.

2 Reports on Progress to Date

2.1 UK institutes

UK groups at the Rutherford Appleton Laboratory and at the University of Birmingham have carried out work on the powering system. Members of the Birmingham and RAL groups have had significant involvement in the development of the power distribution for the upgrade of the ATLAS tracker at the HL-LHC. The expertise includes both the DC-DC based powering scheme adopted by the ATLAS ITk strip detector and the Serial Powering (SP) scheme adopted by the ATLAS ITk pixel detector. Review of these schemes, together with the considerations in the earlier document "Powering options for an EIC silicon tracker" (10.5281/zenodo.6514523), suggests that SP would be the most promising option to reduce material. This scheme is in fact preferred in the upgraded pixel detector not only of ATLAS, but also CMS. In order to keep SP as a viable candidate for the EIC, work has started towards the design of an integrated Shunt-LDO regulator prototype. The first aspect of this, a bandgap circuit, is almost completed.

A powering scheme based on the family of DC-DC buck converters developed at CERN remains a candidate scheme for the EPIC silicon vertex and tracker detector, particularly appealing for the readiness of the converter and the simpler architectural implementation with respect to serial powering. One concern with this approach is the material introduced by the converter itself, in particular the air coil inductor with the required shielding. Architectural choices for the implementation of this scheme will also need to prevent electromagnetic interference with detector modules that would lead to increased noise.

An alternative approach to DC-DC conversion would be the use of on-chip, integrated switch capacitor DC-DC converters. This approach was also considered initially for the ATLAS ITk pixel detector and a converter with a conversion factor 4 was successfully prototyped. Exploring the design of such a converter in the 65 nm CMOS imaging technology chosen for the sensor, will be part of the FY23 proposal in collaboration with eRD113. The aim is to understand the achievable conversion factor and thus the potential for material reduction. If significant, this solution would provide an easier to implement scheme than SP, with less material than the DC-DC buck converter approach.

We note here that the designing of the integrated regulator circuit blocks is part of the eRD113, while the architectural studies are carried out within eRD104.

2.2 Oak Ridge National Laboratory

The ORNL Relativistic Nuclear Physics group (RNP) carried out work on readout services reduction. The ORNL RNP was responsible for the front end electronics of the ALICE TPC upgrade and was significantly contributing to the development of the readout electronics of the ALICE ITS upgrade, both recently completed and now taking data in LHC Run-3. The ITS upgrade is based on the ALPIDE MAPS detector which is the predecessor of the current ITS3 sensor development considered as the technology for the ePIC MAPS tracker.

The initial work on the readout part of the proposal concentrated on fact finding for the proposed ePIC MAPS detector development as well as a market survey of available components for a possible MUX board that uses data aggregation on or close to the detector using radiation tolerant FPGAs to receive multiple data streams from sensor blocks (over Twinax cables or directly from the detector interface area Flexible Printed Circuit (FPC) board), and multiplexes and transmits the data out via high-speed fibers or fiber ribbon connections to intermediate data collection boards or directly to the Data Aggregation Modules (DAM) boards in the ePIC DAQ proposal. The likely candidate for the DAM board in the ePIC proposal is the FELIX board currently proposed for Phase-2 upgrade of ATLAS. The final R&D goal is to develop a MUX board that allows steering control and configuration towards the sensors, as well as aggregate data from the sensors.

Findings of our investigations so far include the following:

- The tracking detector is still evolving, so a final count of the number and speed of readout links from the sensors is not yet complete. With the current design within the ePIC tracking group, the MAPS part of the tracker will install about 9 m^2 of ITS3 type MAPS sensors in the vertex layers, sagitta layers, as well as in the forward and backward barrel regions

- Using the pixel pitch considered by ITS3 sensor developers, this results in a total of about 40.5 Gigapixels.

- Detector simulations with Pythia in GEANT4 result in about 70 hits per event. It is estimated that hits from beam-gas background, synchrotron radiation and others contribute about as much per event. The ITS3 sensor will likely collect the charges from a hit in one pixel, so the total number of pixels firing per event is about 150. The event rate in the EIC ePIC detector is expected as high as 500 kHz, so the readout rate expected from physics and background will result in 75 M pixels per second.

- Recent results from tests with the "Digital Pixel Test Structure" (DPTS, one of the first prototype chips from the ITS3 project) show a "Fake Hit Rate" (FHR) of $10^-2/(pixel * sec)$. With 40.5 Giga Pixels in the ePIC MAPS tracker, this would result in a noise rate of about 405 M pixels per second.

- Current estimate for one "stave" of the ITS3 sensor is that we might have up to 8 links capable of readout speeds up to 5 Gbps.

- The encoding on the readout links will likely change from 8b10b to a more efficient and better performing code compatible with FPGA high-speed transceivers (e.g. 64b66b).

- Possible candidate for a radiation tolerant FPGA: Microchip PolarFire FPGA. It contains from 4 to 24 transceiver lanes cable of 250 Mbps up to 12.7 Gbps; from 48K to 481K logic elements; from 3.6 Mb to 33 Mb of RAM.

- Possible candidate for a Rad-Hard optical interconnect: CERN "lpGBT"; for data uplink the lpGBT provides either 5.12 or 10.24 Gbps. To provide controls and configuration, it provides 2.56 Gbps downlink speed.

- Possible candidate for the electrical/optical interface: Samtec optical "Fire-Fly". One MTP connector on the optical side can provide up to 28 Gbps with x4 and x12 lane designs over OM3 multi-mode fiber. The fiber interconnect can be provided over an MPO high-density connector with up to 24 fibers. The connector takes as little as 0.63 square inches on a PCB, making it possible to keep the MUX board relatively small.

2.3 Brookhaven National Laboratory

Seizing from synergistic, to some extent, material minimization requirements that can be used to build transmission lines between what is necessary, e.g. for reading lXe TPC in the nEXO experiment and for handling data flows from MAPS detectors in the EIC, BNL has started research on the development of data links, in which the transmitter implemented on an integrated circuit, directly driving the transmission line, has adjustable pre-emphasis to a much greater extent than in typical commercial solutions. It is a pre-emphasis control with a sub-symbol time resolution and a pre-emphasis amplitude comparable to or greater than the same amplitude of the transmitted symbols to optimize

data transmission over high insertion loss transmission lines. Such lines with a high value of the insertion loss coefficient are, for example, coplanar transmission lines, implemented on flexible substrates, where the amount of copper is significantly reduced, and these lines are characterized by high attenuation resulting from the dominance of the skin effect. Designing integrated circuit blocks allowing for transmission at speeds of up to a few Gbps using adjustable pre-emphasis is part of the eRD113, where the conversion of such a designed block to TPSCO 65 nm takes place.

As part of eR104, BNL began work on concentrating many data links transmitting at speeds up to a few Gbps, coming from transmitters characterized by a high degree of selection of pre-emphasis parameters and transmitting on transmission lines with a reduced amount of conductor, which could be plugged into ordinary differential inputs of FPGAs. Such common FPGA inputs can be configured to receive differential signals, but are internally not associated with SERDES block queues, which means that there are many more of these ordinary inputs than those intended for transmission by default. Thus, cheaper, and less resourceful FPGAs could be used for data concentration and more connections could be concentrated in a single FPGA, assuming transmission under the indicated conditions would be successful. That would ultimately pay off in reducing the resources needed to collect data. Thus, the work of BNL is aimed at demonstrating this.

3 Deliverables and Milestones

The deliverables and milestones for FY23 include the rollover of the FY22 milestones with expansion to account for the accelerated timeline in preparation for the project TDR. Milestone dates are based on a start date of December 2022. Institutional participation in eRD104 is given in Table 1.

Table 1: Institutions involved and institutional contacts

Topic	**Institute**	**Institutional contact**
Powering System	Birmingham	Laura Gonella
	RAL	Fergus Wilson
Readout System	ORNL	Jo Schambach
	BNL	Grzegorz Deptuch

3.1 Powering

As the detailed concept of the ePIC silicon vertex and tracking detector is evolving, powering architectures based on DC-DC conversion and serial powering will be defined with an analysis of architectural benefits/weaknesses, work needed to complete R&D, material budget and cost, to guide the choice of the most suitable powering scheme for the ePIC detector. In parallel, characterisation of existing DC-DC and SP regulators will be carried out and simple test

benches will be developed to evaluate the performance of existing 65 nm MLR1 test structures powered through those. This will inform the requirements for the regulator as well as initial module/system level considerations. Work in eRD104 will be complemented by the design of integrated power regulators in eRD113. To summarize, the deliverables and milestones for this funding period are:

- **Deliverable:** Detailed concept and analysis of powering distribution schemes based on DC-DC and SP.
  Milestone: Report on powering schemes architectures.
  Deadline: May 2023.

- **Deliverable:** Evaluation of existing regulators and of MLR1 structures performance powered through those.
  Milestone: Report on powering tests with existing regulators.
  Deadline: September 2023.

3.2 Readout

With the various options identified for components of a radiation tolerant FPGA based multiplexing board, the emphasis of this proposal period will be to investigate these components with evaluation boards and combine them in a prototype system as a basis for final board design. As shown above, radiation tolerant FPGAs from Microchip provide high-speed links with speeds on the order of 10 Gbps per transceiver, with multiple transceivers available depending on the specific model of the PolarFire FPGAs. It is not quite clear yet what the readout links for the final ITS3 MAPS sensors will look like and what speed they will provide. The current ALPIDE sensor provides data links with speeds up to 1.2 Gbps. For these speeds it would be possible to multiplex 8 or 9 data links on to one FPGA transceiver link. The downlink communication is much less demanding, for the current ALPIDE the control and trigger links are running at 40 MHz, so this presents no restriction on the bandwidth available in the PolarFire transceivers to multiplex the same amount of control links on the ALPIDE sensor. In private conversation with the chip designers, it was mentioned that the eventual readout of the inner barrel ITS3 sensors (half of an inner layer cylinder) might contain up to 24 readout links with speeds up to 5 Gbps. At that speed one can still multiplex 2 of these links into one transceiver. The VTRx+ module from CERN then further combines 4 TX channels and 1 RX channel into one MTP fiber cable bundle, thus allowing for yet another size reduction from multiple copper cables on the sensor side to 1 (small) fiber bundle with a single MTP connector on the end. While the VTRx+ module has the advantage of being designed radiation tolerant, commercial offerings like the optical Firefly cable from Samtec provides up to 12 fibers in one MTP connector and could provide an alternative to the VTRx+ with even higher

compactness, if it will be fault tolerant enough in the radiation environment. The plan for this proposal period is therefore to obtain evaluation boards of the various components mentioned, develop prototype firmware to multiplex both up and downlink signals to and from either an existing ALPIDE sensor or an FPGA simulating the data and control of a sensor, and investigate all the issues associated with this approach, and possibly test the radiation tolerance of the complete system in a beam test setup. To summarize, the deliverables for this funding period are:

- **Deliverable:** Explore radiation tolerant FPGA options with FPGA evaluation boards.
- **Deliverable:** Explore various high speed fiber optic transmission options (e.g. VTRx+ with lpGBT as a serializer, i.e. VLDB+ with VTRx+, or Samtec optical FireFly) with evaluation boards.
- **Deliverable:** Design and fabricate FMC interface boards for the above evaluation boards.
- **Deliverable:** Develop prototype multiplexing firmware.
- **Deliverable:** Beam tests for fault testing of FPGA evaluation board with fiber optic transmission.
  Milestone: Report on test beam results.
  Deadline: August 2023.
- **Deliverable:** Analysis of multiplexing designs and full cost benefit report.
  Milestone: Report on MUX architectures.
  Deadline: September 2023.

In addition to this approach, an alternative readout scheme will be investigated with the plan to build a subsection of an acquisition system mimicking the one from ALICE ITS2, but based on integrated transmitters, cables on a flexible substrate and the use of FPGA logic inputs without SERDES to reduce costs of FPGA based data receivers as a target for reduced resources, vide cost for the EIC solution.

- **Deliverable:** Development and test of data transmission on high insertion loss cables with adjustable pre-emphasis integrated lines drivers and FPGA differential I/Os.
  Milestone: Report on data transmission tests.
  Deadline: September 2023.

4 FY23 request

The budget for FY23 is split between in kind contributions and funding requested from the project as shown below. Table 2 lists known in-kind contributions. Table 3 presents the costs associated with the FY23 funding request. The corresponding FTE and brief justification are discussed below.

Table 2: Known in-kind contributions [FTE]

Institute	**staff**	**eng**	**tech**	**M&S**
UK groups	0.3	0.2		6k
ORNL	0.2			

Table 3: Total funding request and breakdown by institution. All costs in k$.

Institute	**staff**	**eng**	**tech**	**M&S**	**travel**	**total FY23**
BNL		102	20	16		
ORNL		94.5		16	7	
Total		**196.5**	**20**	**32**	**7**	**255.5**

UK contribution:
Staff (development of architectural concepts for power distribution): **0.3 FTE**.
Electronics engineer (test bench design, regulators testing): **0.2 FTE**.
M&S (PCB, cables): **6k$**.
Note that the UK contribution is in kind on a best effort basis - not costed to project. The UK contribution is funded via the UKRI-STFC Infrastructure Bid for EIC R&D.

ORNL contribution:
Staff: **0.2 FTE**, ORNL in kind contribution.
Electronics Engineer (design of interface boards): **0.15 FTE**.
Mechanical Engineer (design beam test structure): **0.1 FTE**.
M&S (evaluation boards, interface boards, cables, beam test structures): **$16k**
Travel (2 people, 1 week for beam test): **$7k**

BNL contribution:
Electronics Engineer (design of interface boards, testing and characterisation, writing report); **0.25 FTE**.
Technician (board assembly); **0.07** FTE.
M&S (evaluation boards, interface boards, flex-substrate cables with coplanar transmission lines): **$16k**